modified to denote that data DD <15:0> is provided to the data bus from the receive unit 54. This has support, for e.g., on page 16, lines 10-12, where it is indicated that the shift registers of the receive unit store data in parallel to the data bus.

Applicant respectfully requests the Examiner to approve this change to the drawings.

Rejections Under 35 U.S.C. §102

Claims 1-2 and 16-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Walters (U.S. Patent No. 4,408,272). Applicant traverses.

Independent claims 1 and 16 recite in part "a clock signal generator generating a clock signal in response to a mode signal, said mode signal indicating operation in one of at least a first and second data length transfer mode" (emphasis added). Walters fails to suggest, much less disclose, at least this claimed feature.

More specifically, Walters discloses that the following clock signals are generated by the device based on external clock sources. First, the shift register gate 30 generates signal SR CLK 32; the clock/sync generator 28 generates a signal CLOCK 29; and the interval counter gate 40 generates a CNTR CLK 48 (see Figs. 1 and 10). However, none of the shift register gate 30, the clock/sync generator 28, and the interval counter gate 40 generates the respective signals based on the length of data.

In the Office Action, it is correctly noted that parameters L1, L0 of the control register 37 indicate the length of data (see column 3, line 21-24 and column 7, lines 38-42). However, none of the internal clock signals are generated in response to the parameters L1, L0. For example, the shift register gate 30 generates the SR CLK signal primarily based on parameters X, F1, and F0 (see Fig. 3, column 5, line 66 to column 6, line 3; column 7, lines 42-48; column 8, lines 24-28). The signal SR CLK is not generated in response to parameters L1, L0.

Similarly, the clock/sync generator 28 generates sync signal 45 and clock signal 29 in response to parameters F1 and X (see Fig. 7). Parameters L1, L0 play no role in generating these signals.

Further, in the interval counter gate 40, none of the parameters contained in the control register 37 play any direct role in generating the CNTR CLK signal 48.

The length parameters L1, L0 merely serve to indicate the number of times the data in the shift register 20, 120 are to be shifted. Thus, Walters fails to disclose or suggest at least a clock signal generator generating a clock signal in response to a mode signal, as claimed in independent claims 1 and 16. Therefore, the independent claims are not anticipated or rendered obvious by Walters.

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Claims 2 and 17 depend from independent claims 1 and 16. Therefore, these dependent claims are also not anticipated or rendered obvious by Walters for at least the reasons stated with respect to claims 1 and 16.

Applicant respectfully requests the Examiner to withdraw this Section 102 rejection of claims 1-2 and 16-17 based on Walters.

Rejections Under 35 U.S.C. §103

Claims 3-15 and 18-32 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Walters in view of the Related Art described in the specification. Applicant traverses.

Claims 3-15 and 18-32 depend from independent claims 1 and 16, and the independent claims recite in part "a clock signal generator generating a clock signal in response to a mode signal, said mode signal indicating operation in one of at least a first and second data length transfer mode" (emphasis added). It has been shown above that Walters does not disclose or suggest at least this claimed feature. The Related Art fails to cure at least this deficiency of Walters.

It is clear that the Related Art does not disclose or suggest a clock signal generator generating a clock signal in response to a mode signal since the Related Art does not even contemplate transferring data of different lengths. In other words, the data length, as described in the Related Art, is fixed. Thus,

the Related Art does not disclose or suggest the above-recited feature of the independent claims.

Because neither Walters nor the Related Art discloses or suggests a clock signal generator generating a clock signal in response to a mode signal, the mode signal indicating operation in one of at least a first and second data length transfer mode, as claimed above, the combination of Walters and the Related Art also fails to disclose or suggest the above-recited feature. Therefore independent claims 1 and 16 are not rendered obvious by the combination of Walters and the Related Art. It then follows that dependent claims 3-15 and 18-32 are also not rendered obvious by the combination of Walters and the Related Art for at least the reasons stated with respect to independent claims 1 and 16.

In the alternative, claims 3-4 and 18-19 recite in part "the clock signal generator generates a mod 3 clock signal when the mode signal indicates the first data length and generates a mod 4 clock signal when the mode signal indicates the second data length." Neither Walters nor the Related Art discloses or suggests at least this claimed feature.

Regarding Walters, it has been demonstrated above that Walters does not disclose a clock signal generator generating a clock signal in response to a mode signal. If the device, as disclosed in Walters, cannot generate a clock signal based on the mode signal, the device cannot generate any specific clock signal such as a mod 3 or a mod 4 signal in response to the mode signals as

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well. Further, Walters does not even disclose an element that can perform a mod 3 or a mod 4 function. Thus, Walters cannot disclose or suggest the clock signal generating a mod 3 clock signal when the mode signal indicates the first data length and generating a mod 4 clock signal when the mode signal indicates the second data length, as claimed above.

Regarding the Related Art, it has been shown above that the Related Art does not even contemplate transferring data of different data lengths. Therefore it does not contemplate a mode to indicate different data length transfers, and thus cannot disclose or suggest any clock generating circuit generating a clock signal in response to the mode signal, let alone any specific clock signal such as a mod 3 or a mod 4 signal.

Because neither Walters nor the Related Art discloses or suggests at least the above-recited feature of claims 3-4 and 18-19, the combination of Walters and the Related Art also fails to disclose or suggest at least the same feature.

For at least these reasons, dependent claims 3-15 and 18-32 are not rendered obvious by the combination of Walters and the Related Art.

Applicant respectfully requests the Examiner to withdraw this Section 103 rejection of claims 3-15 and 18-32 based on Walters and the Related Art.

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New Claims

By this Amendment, claims 33-34 have been added. These claims depend from independent claims 16 and 17, and therefore are allowable for at least the reasons stated with respect to the independent claims.

In the alternative, claim 33 recites in part "wherein the amount of time spent converting the serial data into parallel data for both the first and second data lengths is constant" (emphasis added). Claim 34 recites similar feature. Neither Walters nor the Related Art discloses or suggests at least this feature.

Walters discloses that the clock SR CLK is enabled to transmit clock pulses to the shift register for a certain number of counts and then the pulses are disabled (see column 8, lines 24-44). Presumably the number of pulses enabled correspond to the data length of the data being shifted.

However, there is no indication that during the time the pulses are enabled, the speed of the pulses being transmitted is varied. It then follows that transmitting data of different lengths will require different amounts of time. For example, it would be logical to assume that transferring 16 bits of data will take twice as long as transferring 8 bits.

Regarding the Related Art, it is clear that the Related Art cannot disclose or suggest the feature as claimed above since it does not even contemplate data transfers of different length.

Because neither Walters nor the Related Art discloses or suggests the feature of claims 33 and 34, these claims are not anticipated either Walters or

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the Related Art and are not rendered obvious by the combination of Walters and the Related Art.

Applicant respectfully requests the Examiner to allow these claims.

CONCLUSION

For the foregoing reasons, Applicant(s) respectfully request(s) the Examiner to withdraw all of the objections and rejections.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Hyung Sohn (Registration No. 44,346) at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment from or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, the extension of time fees.

Respectfully submitted,

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